

WHAT IS CLAIMED IS

1. A programmable logic device comprising:
a programmable logic block operable to provide
5 logical outputs at its output terminals from logical
inputs received at its input terminals; and
a hardwired microsequencer coupled to the input
and output terminals of the programmable logic block,
the microsequencer operable to provide a sequence of
10 logical inputs to the programmable logic block, at
least part of the sequence determined by logical
outputs received from the programmable logic block.
2. The programmable logic device of claim 1,
15 wherein the programmable logic block comprises a
programmable AND array configured to provide a
plurality of product terms based upon a set of logical
inputs and a plurality of macrocells operable to
generate the logical outputs from the product terms.
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3. The programmable logic device of claim 1,
wherein the part of the set of logical inputs provided
to the programmable logic block by the microsequencer
are derived from microinstructions executed by the
25 microsequencer.

4. The programmable logic device of claim 2,
wherein the microinstructions include an input, a jump
destination, and a select command.

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5. The programmable logic device of claim 1,
wherein the microsequencer includes:

a memory configured to store a set of
microinstructions that include logical inputs provided
10 to the programmable logic block; and

a program counter coupled to the memory and
configured to provide addresses to the memory to select
the microinstructions for execution, the program
counter responsive to logical outputs received from the
15 macrocells.

6. The programmable logic device of claim 5,
wherein the program counter is responsive to a jump
destination derived from a previously executed
20 microinstruction.

7. The programmable logic device of claim 5,
wherein the memory is non-volatile.

8. The programmable logic device of claim 5,
wherein the microsequencer includes: a multiplexer
having input terminals for receiving the logical
outputs from the macrocells; an output terminal
5 coupled to the program counter; and a select terminal
coupled to an output terminal of the memory, the
multiplexer responsive to a select command derived from
a previously executed microinstruction.

10 9. A method of sequencing a finite state
machine, comprising:

generating input conditions for a finite state
machine in a programmable logic block based upon a set
of inputs;

15 selecting an input condition from the generated
input conditions based upon a previously-executed
microinstruction selected from a hardwired read-only
memory;

20 selecting a microinstruction from a set of stored
microinstructions in the read-only memory based upon
the selected input condition and the previously-
executed microinstruction; and

executing the selected microinstruction to provide
inputs for the set of inputs.

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10. The method of claim 9, wherein the selecting
a microinstruction act comprises:

if the selected input condition is in a first
binary state, selecting the microinstruction at a jump
5 destination derived from the previously-executed
microinstruction; and

if the selected input condition is complementary
to the first binary state, selecting the
microinstruction according to a predetermined
10 microinstruction sequence.

11. The method of claim 10, wherein the executing
the microinstruction act includes determining the first
binary state.

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12. The method of claim 9, wherein the
programmable logic block comprise a programmable AND
array, and the generating input conditions act
comprises processing product terms through the
20 programmable AND array.

13. A programmable logic device, comprising:
a logic block operable to provide input conditions
for a finite state machine based upon a set of inputs;
25 and

a hardwired microsequencer configured to determine a next state of the finite state machine by cyclically executing a microinstruction selected from a set of microinstructions responsive to cycles of a system
5 clock, wherein at a given cycle of the system clock, the executed microinstruction depends upon the previously-executed microinstruction and an input condition selected from the input conditions provided by the logic block, and wherein the set of inputs for
10 the logic block includes inputs derived from the executed microinstruction.

14. The programmable logic device of claim 13, wherein the hardwired microsequencer includes:

15 a sequence memory configured to store the set of microinstructions; and

a program counter configured to determine the microinstruction to be executed at each internal clock cycle, wherein depending upon the selected input
20 condition, the program counter determines the microinstruction either according to a predetermined sequence of the microinstructions or to a jump destination derived from the previously-executed microinstruction.

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15. The programmable logic device of claim 14,
wherein the sequence memory is a read-only memory.

16. The programmable logic device of claim 14,
5 wherein the sequence memory is a non-volatile
electrically-alterable read-only memory.

17. The programmable logic device of claim 14,
wherein the hardwired microsequencer further includes a
10 multiplexer configured to select from the input
conditions provided by the logic block and determine
the selected input signal according to a condition
selection command derived from the previously-executed
microinstruction.

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18. The programmable logic device of claim 14,
wherein the program counter is configured to determine
the microinstruction according to the jump destination
if the selected input condition is in a first binary
20 state and wherein the program counter is configured to
determine the microinstruction according to the
predetermined sequence if the selected input condition
is in the complementary binary state to the first
binary state

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19. The programmable logic device of claim 18,
wherein the first binary state is determined by the
previously-executed microinstruction.

5 20. The programmable logic device of claim 18,
wherein the hardwired microsequencer further includes:
a multiplexer configured to select from the input
conditions provided by the logic block and determine
the selected input signal according to a condition
10 selection command derived from the previously-executed
microinstruction; and
an exclusive OR gate configured to receive the
selected input signal from the multiplexer and a binary
state selection command derived from the previously-
15 executed microinstruction to determine the first binary
state.